IN THE CLAIMS

Please cancel claims 1-11.

Please amend claim 12. All currently pending claims and status indicators are set forth below.

12. (Currently Amended)   A method of resynchronizing a memory system, comprising the acts of:

       initiating a first refresh request to each of a plurality of semiconductor

            memory segments in a memory system while the memory system is

            operating in a non-redundant mode;

       waiting a number of clock cycles after initiating the first refresh request; ~~and~~

       initiating a second refresh request to each of the plurality of memory segments

            and;

       transitioning the computer system to a redundant mode of operation.

13. (Original) The method, as set forth in claim 12, wherein the act of initiating a first refresh request comprises the acts of:

       initiating a resynchronization command from a host controller to each of a

            plurality of memory controllers, wherein each of the plurality of

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memory controllers provides access to a respective one of the plurality

of memory segments; and

deactivating a refresh counter in each of the memory controllers, wherein the

act of deactivating the refresh counter generates the first refresh

request.

14. (Original) The method, as set forth in claim 13, wherein if the refresh counter is

executing a current refresh command when the resynchronization command is received, the

refresh command generated by the act of deactivating the refresh counter is ignored by the

respective memory controller.

15. (Original) The method, as set forth in claim 13, comprising the act of resetting

state machines in each of the plurality of memory controllers in response to the act of

initiating the resynchronization command.

16. (Original) The method, as set forth in claim 13, comprising the act of resetting

arbiters in each of the plurality of memory controllers in response to the act of initiating the

resynchronization command.

17. (Original) The method, as set forth in claim 12, wherein the act of waiting a

number of clock cycles comprises the act of waiting until each first refresh request has

completed execution.

18. (Original) The method, as set forth in claim 12, wherein the act of waiting a number of clock cycles comprises the act of waiting at least 15 clock cycles.

19. (Original) The method, as set forth in claim 12, wherein the act of initiating a second refresh request comprises the act of re-activating a refresh counter in each of the memory controllers, wherein the act of re-activating the refresh counter generates the second refresh request.

20. (Original) A method of resynchronizing a semiconductor memory system, comprising the acts of:

> initiating a resynchronization command to each of a plurality of memory
>> cartridges;
> disabling a refresh counter in each of the plurality of memory cartridges; and

> enabling the refresh counter in each of the plurality of memory cartridges.

21. (Original) The method, as set forth in claim 20, wherein the act of initiating comprises the act of initiating a resynchronization command from a host controller.

22. (Original) The method, as set forth in claim 20, comprising the act of resetting state machines in each of the plurality of memory controllers in response to the act of initiating the resynchronization command.

23. (Original) The method, as set forth in claim 20, comprising the act of resetting arbiters in each of the plurality of memory controllers in response to the act of initiating the resynchronization command.

24. (Original) The method, as set forth in claim 20, wherein the act of disabling comprises the act of initiating a first refresh request from the refresh counter to a plurality of memory devices on each of the plurality of memory cartridges.

25. (Original) The method, as set forth in claim 20, wherein the act of enabling comprises the act of initiating a second refresh request from the refresh counter to a plurality of memory devices on each of the plurality of memory cartridges.

26. (Original) The method, as set forth in claim 20, comprising the act of waiting a number of clock cycles between the act of disabling the refresh counter and the act of enabling the refresh counter.

27. (Original) The method, as set forth in claim 26, wherein the act of waiting comprises the act of waiting at least 15 clock cycles between the act of disabling the refresh counter and the act of enabling the refresh counter.

28. (Original) A memory system comprising:

    a plurality of semiconductor memory segments; and

a plurality of memory controllers, wherein each of the plurality of memory

controllers is coupled to a respective one of the plurality of memory

segments, each of the plurality of memory controllers comprising a

refresh counter configured to facilitate the synchronization of each of

the memory segments with respect to one another.

29. (Original) The memory system, as set forth in claim 28, wherein each of the

memory segments comprises a plurality of dual inline memory modules (DIMMs).

30. (Original) The memory system, as set forth in claim 28, wherein each of the

plurality of memory controllers is configured to receive a resynchronization command from a

host controller.

31. (Original) The memory system, as set forth in claim 30, wherein each refresh

counter is configured to be disabled in response to receiving the resynchronization command.

32. (Original) The memory system, as set forth in claim 31, wherein each refresh

counter is configured to generate a first refresh request to the respective memory segment in

response to being disabled.

33. (Original) The memory system, as set forth in claim 32, wherein each refresh

counter is configured to be enabled at some number of clock cycles after the

resynchronization command.

34. (Original) The memory system, as set forth in claim 33, wherein each refresh counter is configured to generate a second refresh request to the respective memory segment in response to being enabled.

35. (Original) The memory system, as set forth in claim 28, wherein each of the plurality of memory controllers comprises a plurality of state machines and arbiters.

36. (Original) The memory system, as set forth in claim 35, wherein each of the plurality of state machines is configured to be reset in response to receiving a resynchronization command.

37. (Original) The memory system, as set forth in claim 35, wherein each of the plurality of arbiters is configured to be reset in response to receiving a resynchronization command.

38. (Original) A system comprising:

a host controller;

a plurality of semiconductor memory segments operably coupled to the host controller; and

a plurality of memory controllers, wherein each of the plurality of memory controllers is coupled to a respective one of the plurality of memory segments, each of the plurality of memory controllers comprising a

refresh counter configured to facilitate the synchronization of each of the memory segments with respect to one another.

39. (Original) The system, as set forth in claim 38, wherein the host controller is configured to initiate a resynchronization command to each of the plurality of memory controllers.

40. (Original) The system, as set forth in claim 38, wherein each of the memory segments comprises a plurality of dual inline memory modules (DIMMs).

41. (Original) The system, as set forth in claim 39, wherein each refresh counter is configured to be disabled in response to receiving the resynchronization command.

42. (Original) The memory system, as set forth in claim 41, wherein each refresh counter is configured to generate a first refresh request to the respective memory segment in response to being disabled.

43. (Original) The memory system, as set forth in claim 42, wherein each refresh counter is configured to be enabled at some number of clock cycles after the resynchronization command.

44. (Original) The memory system, as set forth in claim 43, wherein each refresh counter is configured to generate a second refresh request to the respective memory segment in response to being enabled.

45. (Original) The memory system, as set forth in claim 39, wherein each of the plurality of memory controllers comprises a plurality of state machines and arbiters.

46. (Original) The memory system, as set forth in claim 45, wherein each of the plurality of state machines is configured to be reset in response to receiving a resynchronization command.

47. (Original) The memory system, as set forth in claim 45, wherein each of the plurality of arbiters is configured to be reset in response to receiving a resynchronization command.

48. (Original) A method of hot-plugging a semiconductor memory segment into an operating memory system, the method comprising the acts of:

inserting a memory segment into an operating memory system having a plurality of memory segments;

synchronizing the inserted memory segment with the plurality of memory segments; and

operating the memory system with the inserted memory segment and the plurality of memory segments.

49. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 48, wherein the act of synchronizing comprises the acts of:

initiating a first refresh request to each of the inserted memory segment and the plurality of memory segments;

waiting a number of clock cycles after initiating the first refresh request; and

initiating a second refresh request to each of the inserted memory segment and the plurality of memory segments.

50. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 49, wherein the act of initiating a first refresh request comprises the acts of:

initiating a resynchronization command from a host controller to each of a plurality of memory controllers, wherein each of the plurality of memory controllers provides access to a respective one of the plurality of memory segments; and

deactivating a refresh counter in each of the memory controllers, wherein the act of deactivating the refresh counter generates the first refresh request.

51. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 50, wherein if the refresh counter is executing a current refresh command when the resynchronization command is received, the refresh command generated by the act of deactivating the refresh counter is ignored.

52. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 50, comprising the act of resetting state machines in each of the plurality of memory controllers in response to the act of initiating the resynchronization command.

53. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 50, comprising the act of resetting arbiters in each of the plurality of memory controllers in response to the act of initiating the resynchronization command.

54. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 49, wherein the act of waiting a number of clock cycles comprises the act of waiting until each first refresh request has completed execution.

55. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 49, wherein the act of waiting a number of clock cycles comprises the act of waiting at least 15 clock cycles.

56. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 49, wherein the act of initiating a second refresh request comprises the act of re-activating a refresh counter in each of the memory controllers, wherein the act of re-activating the refresh counter generates the second refresh request.

57. (Original) The method of hot-plugging a semiconductor memory segment, as set forth in claim 48, wherein the act of operating comprises the act of operating the memory system in a redundant mode.